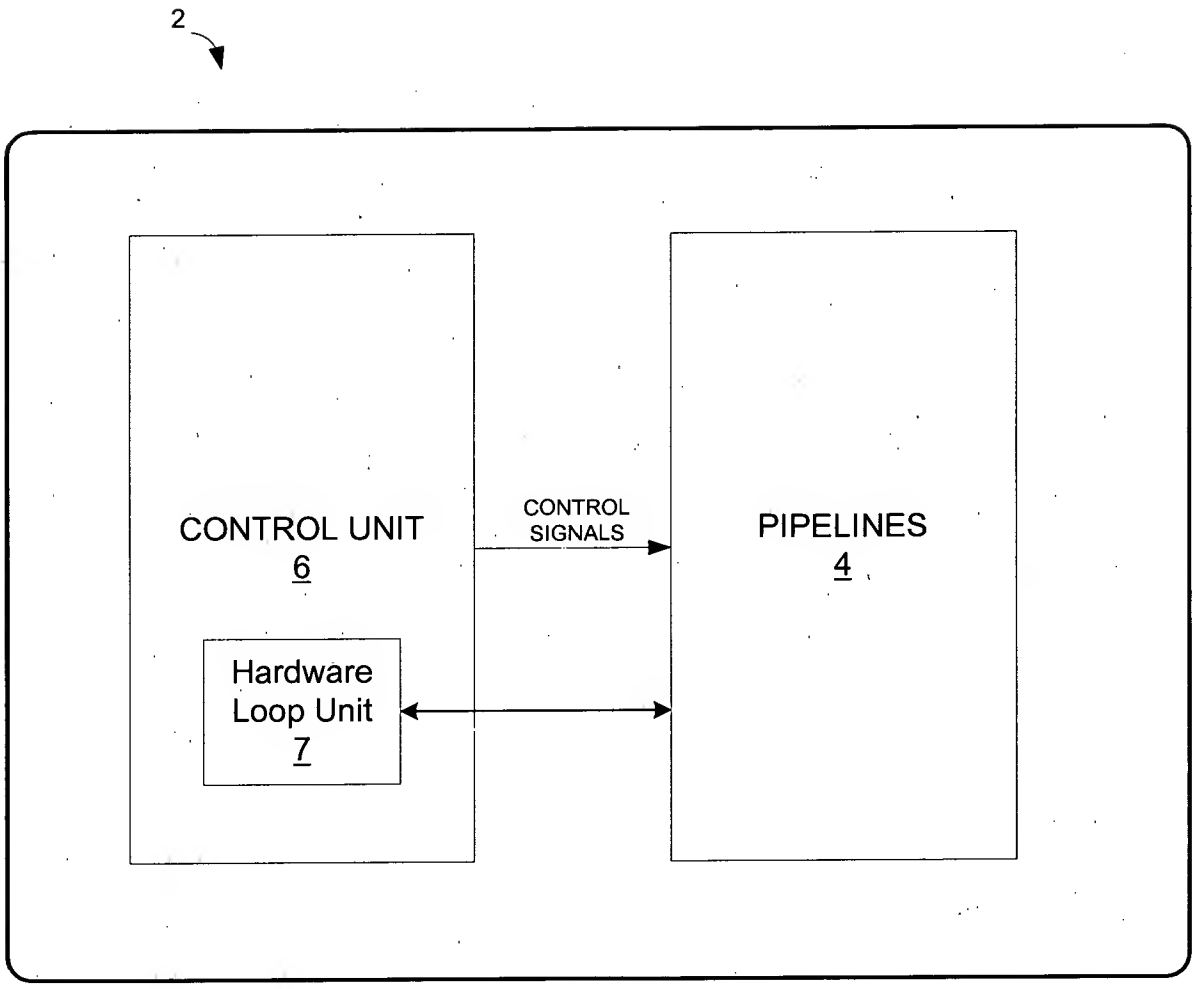
2
CONTROL UNIT
6
Hardware
Loop Unit
7
CONTROL
SIGNALS
PIPELINES
4

FIG. 1

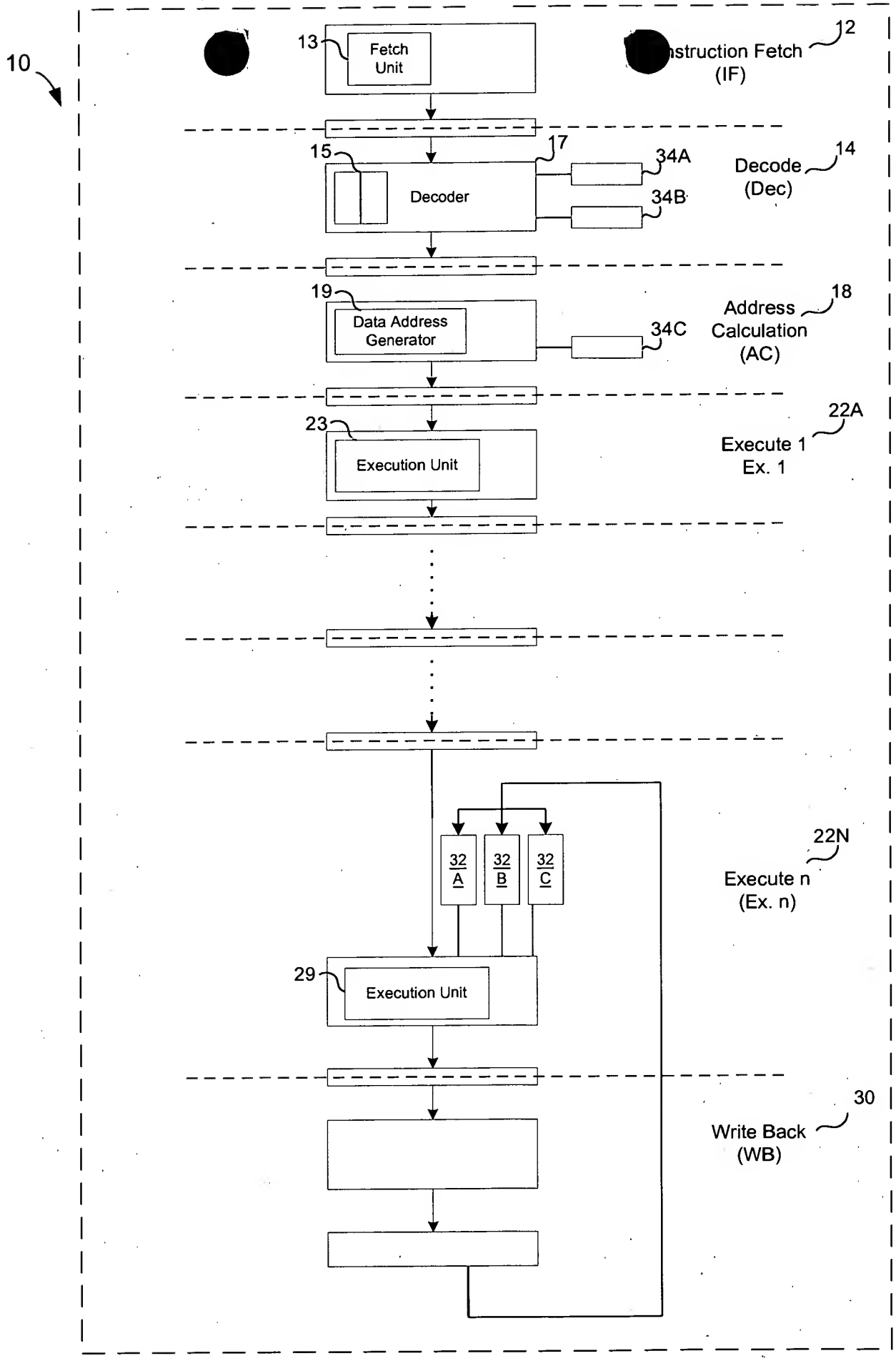
10
13
Fetch Unit
12
Instruction Fetch (IF)
15
17
Decoder
34A
34B
14
Decode (Dec)
19
Data Address Generator
34C
18
Address Calculation (AC)
23
Execution Unit
22A
Execute 1 Ex. 1
32 A
32 B
32 C
22N
Execute n (Ex. n)
29
Execution Unit
30
Write Back (WB)

FIG. 2

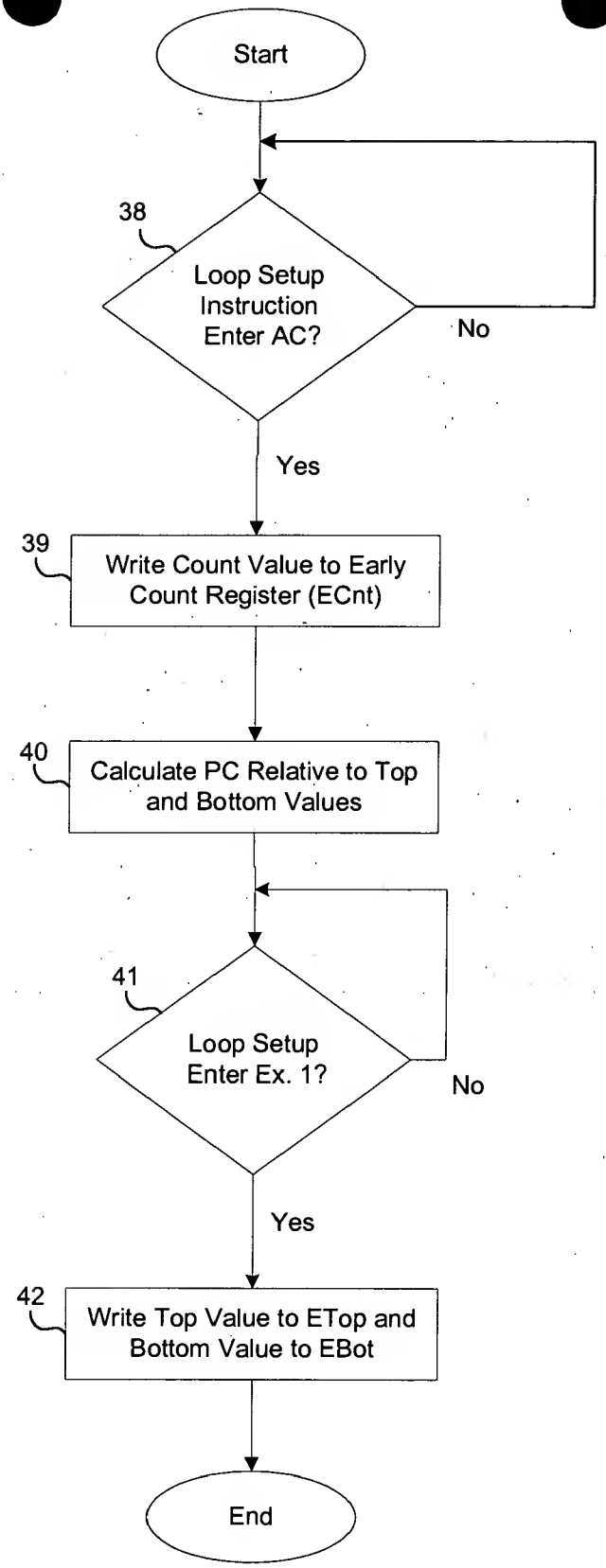
Start
38
Loop Setup Instruction Enter AC?
No
Yes
39
Write Count Value to Early Count Register (ECnt)
40
Calculate PC Relative to Top and Bottom Values
41
Loop Setup Enter Ex. 1?
No
Yes
42
Write Top Value to ETop and Bottom Value to EBot
End

FIG. 3

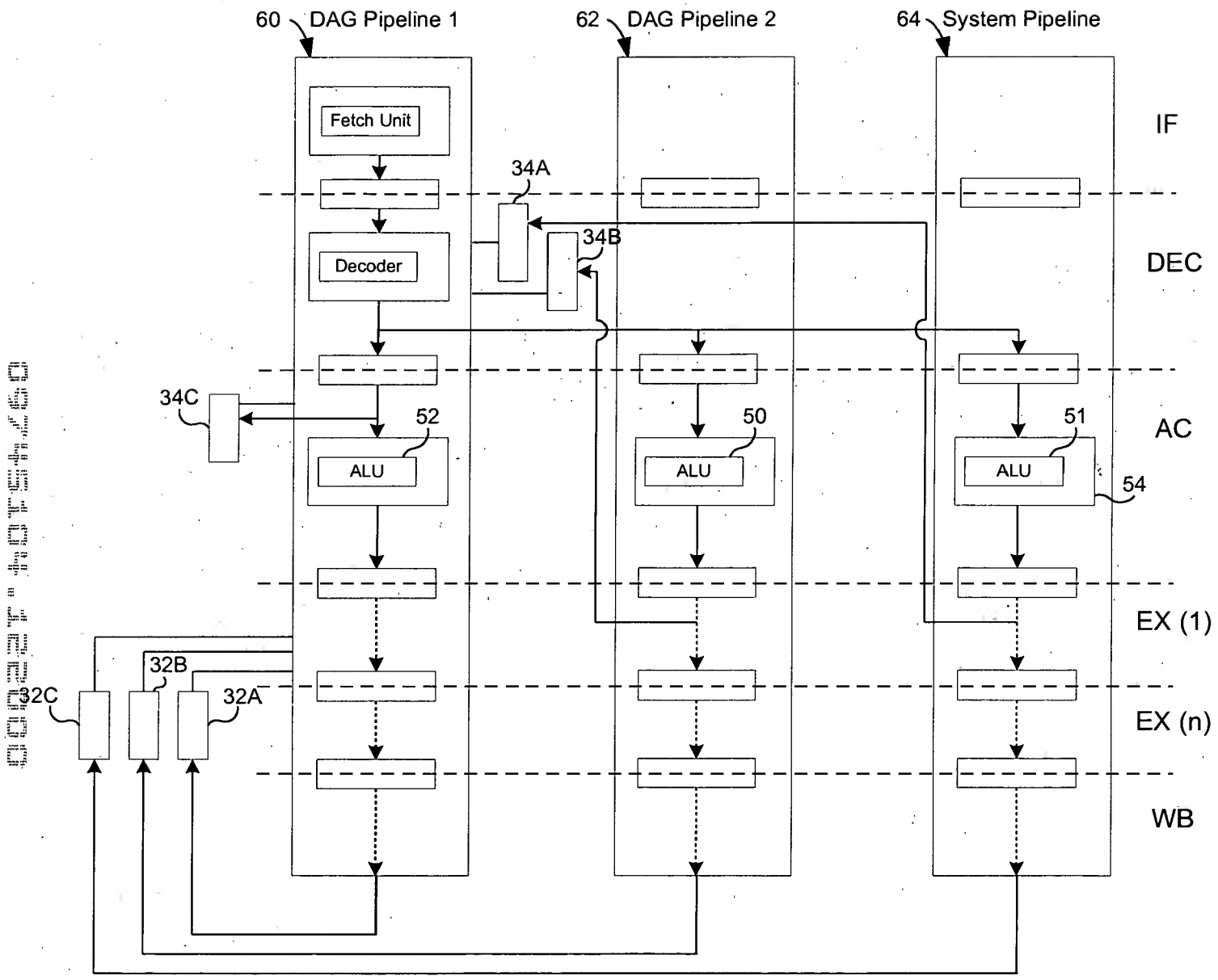
60 DAG Pipeline 1
62 DAG Pipeline 2
64 System Pipeline
Fetch Unit
Decoder
ALU
ALU
ALU
34A
34B
34C
52
50
51
54
32A
32B
32C
IF
DEC
AC
EX (1)
EX (n)
WB

FIG. 4

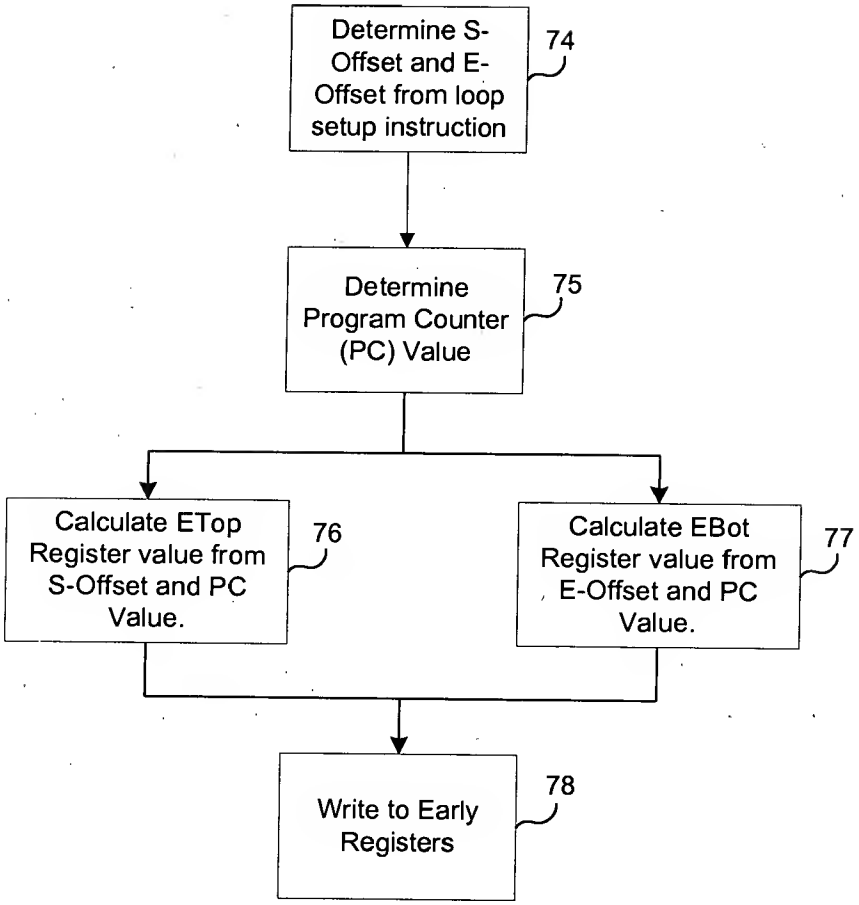
Determine S-Offset and E-Offset from loop setup instruction
74
Determine Program Counter (PC) Value
75
Calculate ETop Register value from S-Offset and PC Value.
76
Calculate EBot Register value from E-Offset and PC Value.
77
Write to Early Registers
78

FIG. 5

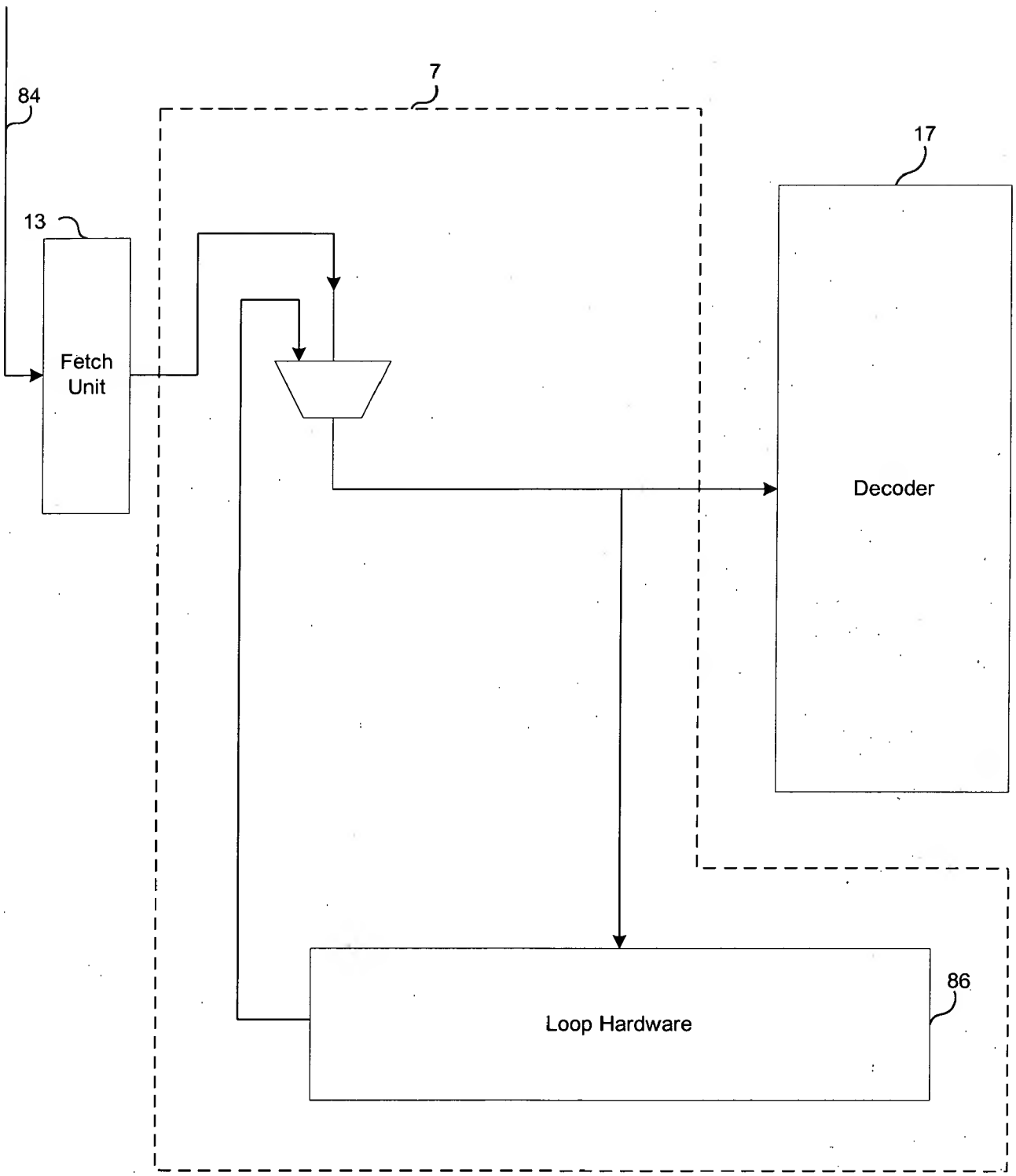

FIG. 6

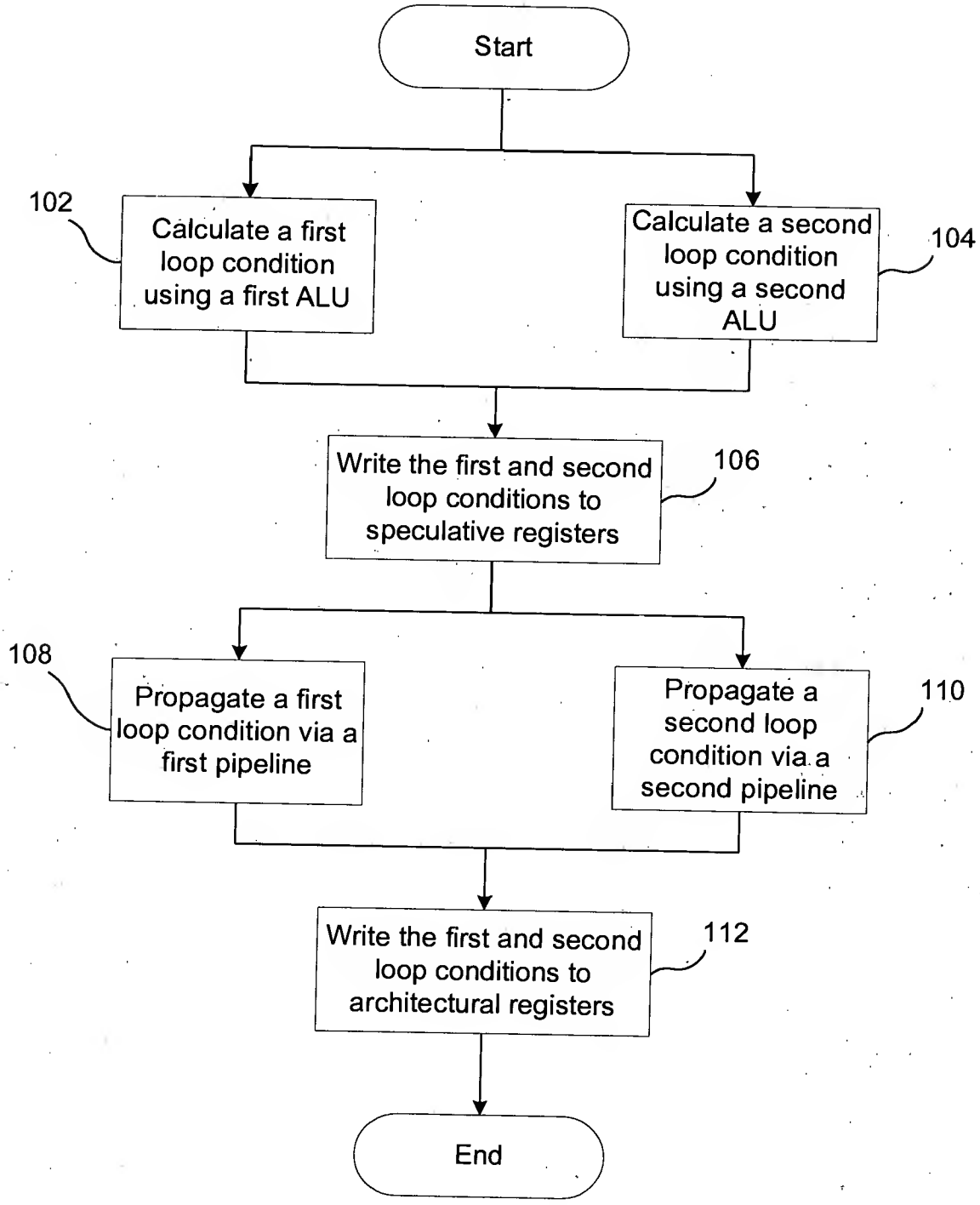
Start
102
Calculate a first loop condition using a first ALU
Calculate a second loop condition using a second ALU
104
Write the first and second loop conditions to speculative registers
106
108
Propagate a first loop condition via a first pipeline
Propagate a second loop condition via a second pipeline
110
Write the first and second loop conditions to architectural registers
112
End

FIG. 7